Search History

STN (USPATALL) 6/14/05

=> d 13 1-12 abs,bib

L3 ANSWER 1 OF 12 USPATFULL on STN

AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:30833 USPATFULL

TI Method for producing insulated gate thin film semiconductor device

IN Kusumoto, Naoto, Kanagawa, JAPAN
Yamazaki, Shunpei, Tokyo, JAPAN

PA Semiconductor Energy Laboratory Co., Ltd., Japanese corporation (non-U.S. corporation)

PI US 2002017649 A1 20020214
US 6709905 B2 20040323

AI US 2001-941366 A1 20010828 (9)

RLI Continuation of Ser. No. US 2001-903339, filed on 10 Jul 2001, PENDING
Continuation of Ser. No. US 1999-375308, filed on 16 Aug 1999, GRANTED, Pat. No. US 6265745 Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, GRANTED, Pat. No. US 5953597

PRAI JP 1995-56481 19950221

DT Utility

FS APPLICATION

LREP SCOTT C. HARRIS, Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA, 92122

CLMN Number of Claims: 24

ECL Exemplary Claim: 1

DRWN 8 Drawing Page(s)

LN.CNT 682

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 2 OF 12 USPATFULL on STN

AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:25782 USPATFULL

TI Method for producing insulated gate thin film semiconductor device

IN Kusumoto, Naoto, Kanagawa, JAPAN
Yamazaki, Shunpei, Tokyo, JAPAN

PA Semiconductor Energy Laboratory Co., Ltd. Japanese corporation (non-U.S. corporation)

PI US 2002014623 A1 20020207

AI US 2001-941367 A1 20010828 (9)

RLI Continuation of Ser. No. US 2001-903339, filed on 10 Jul 2001, PENDING
Continuation of Ser. No. US 1999-375308, filed on 16 Aug 1999, GRANTED, Pat. No. US 6265745 Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, GRANTED, Pat. No. US 5953597

PRAI JP 1995-56481 19950221

DT Utility

FS APPLICATION

LREP SCOTT C. HARRIS, Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA, 92122

CLMN Number of Claims: 20

ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 690
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 3 OF 12 USPATFULL on STN
AB In a method of etching an Al or Al alloy layer, an Al or Al alloy layer is formed on an underlying surface, the surface of the Al or Al alloy layer is processed with TMAH, a resist pattern is formed on the surface of the Al or Al alloy layer processed with TMAH, and by using the resist pattern as an etching mask, the Al or Al alloy layer is wet-etched..

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:1188 USPATFULL
TI Etching method, thin film transistor matrix substrate, and its manufacture
IN Ishida, Yukimasa, Kawasaki, JAPAN
PA Fujitsu Limited, Kawasaki, JAPAN (non-U.S. corporation)
PI US 6335290 B1 20020101
AI US 1999-277791 19990329 (9)
PRAI JP 1998-218063 19980731
DT Utility
FS GRANTED
EXNAM Primary Examiner: Niebling, John F.; Assistant Examiner: Simkovic, Viktor
LREP Greer, Burns & Crain, Ltd.
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 32 Drawing Figure(s); 12 Drawing Page(s)
LN.CNT 1025
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 4 OF 12 USPATFULL on STN
AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:217084 USPATFULL
TI Method for producing insulated gate thin film semiconductor device
IN Kusumoto, Naoto, Kanagawa, Japan
Yamazaki, Shunpei, Tokyo, Japan
PA Semiconductor Energy Laboratory Co., Ltd. (non-U.S. corporation)
PI US 2001045563 A1 20011129
AI US 2001-903339 A1 20010710 (9)
RLI Continuation of Ser. No. US 1999-375308, filed on 16 Aug 1999, GRANTED, Pat. No. US 6265745 Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, GRANTED, Pat. No. US 5953597
PRAI JP 1995-56481 19950221
DT Utility
FS APPLICATION
LREP FISH & RICHARDSON, PC, 4350 LA JOLLA VILLAGE DRIVE, SUITE 500, SAN DIEGO, CA, 92122
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 639
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 5 OF 12 USPATFULL on STN
AB In a method of etching an Al or Al alloy layer, an Al or Al alloy layer is formed on an underlying surface, the surface of the Al or Al alloy

layer is processed with TMAH, a resist pattern is formed on the surface of the Al or Al alloy layer processed with TMAH, and by using the resist pattern as an etching mask, the Al or Al alloy layer is wet-etched.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:149682 USPATFULL
TI Etching method, thin film transistor matrix substrate, and its manufacture
IN Ishida, Yukimasa, Kawasaki-shi, Japan
PA Fujitsu Limited (non-U.S. corporation)
PI US 2001019127 A1 20010906
US 6534789 B2 20030318
AI US 2001-829531 A1 20010409 (9)
RLI Division of Ser. No. US 1999-277791, filed on 29 Mar 1999, PENDING
PRAI JP 1998-218063 19980731
DT Utility
FS APPLICATION
LREP Patrick G. Burns, Greer, Burns & Crain, Ltd., Suite 2500, 300 South Wacker Drive, Chicago, IL, 60606
CLMN Number of Claims: 28
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 1079
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 6 OF 12 USPATFULL on STN
AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:117350 USPATFULL
TI Method for producing insulated gate thin film semiconductor device
IN Kusumoto, Naoto, Kanagawa, Japan
Yamazaki, Shunpei, Tokyo, Japan
PA Semiconductor Energy Laboratory Co., Ltd., Kanagawa-ken, Japan (non-U.S. corporation)
PI US 6265745 B1 20010724
AI US 1999-375308 19990816 (9)
RLI Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, now patented, Pat. No. US 5953597
PRAI JP 1995-56481 19950221
DT Utility
FS GRANTED
EXNAM Primary Examiner: Ngo , Ngan V.
LREP Fish & Richardson P.C.
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 39 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 740
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 7 OF 12 USPATFULL on STN
AB A double level gate layer with an undercut lower gate layer can be formed by using the etching rate difference between the upper gate layer and the lower gate layer in a polycrystalline Si type TFT LCD that has P-channel TFTs and N-channel TFTs. An LDD structure can be easily formed by using an upper gate layer as ion implant mask during the N-type ion implantation. LDD size is decided by the skew size between the upper gate layer and the lower gate layer. Furthermore, a photolithography step necessary for masking the ion implantation can be skipped.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:114516 USPATFULL
TI Method for forming a TFT in a liquid crystal display
IN Lee, Joo-Hyung, Seoul, Korea, Republic of
Hong, Mun-Pyo, Sungnam-shi, Korea, Republic of
Youn, Chan-Joo, Seoul, Korea, Republic of
Jung, Byung-Hoo, Anyang-shi, Korea, Republic of
Hwang, Chang-Won, Sungnam-shi, Korea, Republic of
PI US 2001008781 A1 20010719
US 6403406 B2 20020611
AI US 2001-793541 A1 20010227 (9)
RLI Division of Ser. No. US 1999-323030, filed on 1 Jun 1999, GRANTED, Pat. No. US 6225150
PRAI KR 1998-19760 19980529
KR 1998-48365 19981112
KR 1998-53796 19981208
DT Utility
FS APPLICATION
LREP HOWREY SIMON ARNOLD & WHITE LLP, BOX 34, 1299 PENNSYLVANIA AVENUE NW, WASHINGTON, DC, 20004
CLMN Number of Claims: 14
ECL Exemplary Claim: 1
DRWN 18 Drawing Page(s)
LN.CNT 487
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 8 OF 12 USPATFULL on STN
AB A double level gate layer with an undercut lower gate layer can be formed by using the etching rate difference between the upper gate layer and the lower gate layer in a polycrystalline Si type TFT LCD that has P-channel TFTs and N-channel TFTs. An LDD structure can be easily formed by using an upper gate layer as ion implant mask during the N-type ion implantation. LDD size is decided by the skew size between the upper gate layer and the lower gate layer. Furthermore, a photolithography step necessary for masking the ion implantation can be skipped.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:63527 USPATFULL
TI Method for forming a TFT in a liquid crystal display
IN Lee, Joo-Hyung, Seoul, Korea, Republic of
Hong, Mun-Pyo, Sungnam-shi, Korea, Republic of
Youn, Chan-Joo, Seoul, Korea, Republic of
Jung, Byung-Hoo, Anyang-shi, Korea, Republic of
Hwang, Chang-Won, Sungnam-shi, Korea, Republic of
PA Samsung Electronics Co., Ltd., Seoul, Korea, Republic of (non-U.S. corporation)
PI US 6225150 B1 20010501
AI US 1999-323030 19990601 (9)
PRAI KR 1998-19760 19980529
KR 1998-48365 19981112
KR 1998-53796 19981208
DT Utility
FS Granted
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Nhu, David
LREP Howrey Simon Arnold & White, LLP
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 32 Drawing Figure(s); 18 Drawing Page(s)
LN.CNT 435
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 9 OF 12 USPATFULL on STN
AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel

of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:40314 USPATFULL
TI Method for producing insulated gate thin film semiconductor device
IN Kusumoto, Naoto, Kanagawa, Japan
Yamazaki, Shunpei, Tokyo, Japan
PA Semiconductor Energy Laboratory Co., Ltd., Japan (non-U.S. corporation)
PI US 6204099 B1 20010320
AI US 1999-390904 19990907 (9)
RLI Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, now patented, Pat. No. US 5953597 Continuation of Ser. No. US 1999-375308, filed on 16 Aug 1999
PRAI JP 1995-56481 19950221
DT Utility
FS Granted
EXNAM Primary Examiner: Zarabian, Amir; Assistant Examiner: Lebentritt, Michael S.
LREP Fish & Richardson P.C.
CLMN Number of Claims: 80
ECL Exemplary Claim: 1
DRWN 39 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 845
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 10 OF 12 USPAT2 on STN
AB An amorphous semiconductor film is etched so that a width of a narrowest portion thereof is 100 μm or less, thereby forming island semiconductor regions. By irradiating an intense light such as a laser into the island semiconductor regions, photo-annealing is performed to crystallize it. Then, of end portions (peripheral portions) of the island semiconductor regions, at least a portion used to form a channel of a thin film transistor (TFT), or a portion that a gate electrode crosses is etched, so that a region that the distortion is accumulated is removed. By using such semiconductor regions, a TFT is produced.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:30833 USPAT2
TI Method for producing insulated gate thin film semiconductor device
IN Kusumoto, Naoto, Kanagawa, JAPAN
Yamazaki, Shunpei, Tokyo, JAPAN
PA Semiconductor Energy Laboratory Co., Ltd., Atsugi, JAPAN (non-U.S. corporation)
PI US 6709905 B2 20040323
AI US 2001-941366 20010828 (9)
RLI Continuation of Ser. No. US 2001-903339, filed on 10 Jul 2001 Continuation of Ser. No. US 1999-375308, filed on 16 Aug 1999, now patented, Pat. No. US 6265745 Continuation of Ser. No. US 1996-604547, filed on 21 Feb 1996, now patented, Pat. No. US 5953597
PRAI JP 1995-56481 19950221
DT Utility
FS GRANTED
EXNAM Primary Examiner: Cao, Phat X.; Assistant Examiner: Doan, Theresa T.
LREP Fish & Richardson P.C.
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 39 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 617
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 11 OF 12 USPAT2 on STN
AB Semiconductor islands are formed on an insulating substrate. A gate insulating layer is formed to traverse an intermediate region of each island, and a gate electrode with tapered sidewalls is formed thereon to leave wing-shaped gate insulating layer exposed at both sides. Ion implantation is done to form heavily doped regions in the semiconductor

islands outside the gate insulating layers, and lightly doped drain regions under the wing regions of the gate insulating layer. An interlayer insulating layer is formed thereon to cover the gate electrodes, gate insulating layers, and the semiconductor islands. However, if the gate electrode layer and gate insulating film are patterned in the same shape, a step becomes high. If the wiring area is made narrow, the gate electrode

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:149682 USPAT2
TI Thin film transistor matrix having TFT with LDD regions
IN Ishida, Yukimasa, Kawasaki, JAPAN
PA Fujitsu Limited, Kawasaki, JAPAN (non-U.S. corporation)
PI US 6534789 B2 20030318
AI US 2001-829531 20010409 (9)
RLI Division of Ser. No. US 1999-277791, filed on 29 Mar 1999, now patented, Pat. No. US 6335290
PRAI JP 1998-218063 19980731
DT Utility
FS GRANTED
EXNAM Primary Examiner: Eckert, II, George C.
LREP Greer, Burns & Crain, Ltd.
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 32 Drawing Figure(s); 12 Drawing Page(s)
LN.CNT 1011
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L3 ANSWER 12 OF 12 USPAT2 on STN
AB A double level gate layer with an undercut lower gate layer can be formed by using the etching rate difference between the upper gate layer and the lower gate layer in a polycrystalline Si type TFT LCD that has P-channel TFTs and N-channel TFTs. An LDD structure can be easily formed by using an upper gate layer as ion implant mask during the N-type ion implantation. LDD size is decided by the skew size between the upper gate layer and the lower gate layer. Furthermore, a photolithography step necessary for masking the ion implantation can be skipped.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:114516 USPAT2
TI Method for forming a TFT in a liquid crystal display
IN Lee, Joo-Hyung, Seoul, KOREA, REPUBLIC OF
Hong, Mun-Pyo, Kyunggi-do, KOREA, REPUBLIC OF
Youn, Chan-Joo, Seoul, KOREA, REPUBLIC OF
Jung, Byung-Hoo, Kyunggi-do, KOREA, REPUBLIC OF
Hwang, Chang-Won, Kyunggi-do, KOREA, REPUBLIC OF
PA Samsung Electronics Co., Ltd, Suwon, KOREA, REPUBLIC OF (non-U.S. corporation)
PI US 6403406 B2 20020611
AI US 2001-793541 20010227 (9)
RLI Division of Ser. No. US 1999-323030, filed on 1 Jun 1999, now patented, Pat. No. US 6225150
PRAI KR 1998-19760 19980529
KR 1998-48365 19981112
KR 1998-53796 19981208
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nguyen, Viet Q.; Assistant Examiner: Nhu, David
LREP McGuireWoods LLP
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 32 Drawing Figure(s); 18 Drawing Page(s)
LN.CNT 452
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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      (FILE 'HOME' ENTERED AT 11:42:21 ON 14 JUN 2005)

      FILE 'STNGUIDE' ENTERED AT 11:42:24 ON 14 JUN 2005

      FILE 'USPATFULL, USPAT2' ENTERED AT 11:42:50 ON 14 JUN 2005
L1          3233 S (PATTERN?)(8A)(AMORPHOUS(W)SILICON)
L2            35 S (LASER(4A)CRYSTALIZ?)
L3            12 S L1 AND L2

=>
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Day : Tuesday
Date: 6/14/2005

PALM INTRANET

Time: 10:31:32

Inventor Name Search Result

Your Search was:

Last Name = LIN
First Name = CHING-WEI

Application#	Patent#	Status	Date Filed	Title	Inventor Name 11
60649617	Not Issued	020	02/04/2005	ARCHITECTURE OF OUTPUT STAGE OF DIGITAL-TO-ANALOG CONVERTER	LIN, CHING-WEI
60587660	Not Issued	020	07/13/2004	SHIFT REGISTER	LIN, CHING-WEI
11061836	Not Issued	030	02/18/2005	ANALOG BUFFERS COMPOSED OF THIN FILM TRANSISTORS	LIN, CHING-WEI
10980781	Not Issued	030	11/04/2004	SHIFT REGISTER AND FLAT PANEL DISPLAY APPARATUS USING THE SAME	LIN, CHING-WEI
10968243	Not Issued	030	10/20/2004	ESD PROTECTION CIRCUIT FOR CHARGE PUMP AND ELECTRONIC DEVICE AND SYSTEM USING THE SAME	LIN, CHING-WEI
10935860	Not Issued	030	09/07/2004	METHOD AND CIRCUIT FOR DRIVING LIQUID CRYSTAL DISPLAY	LIN, CHING-WEI
10850320	Not Issued	030	05/19/2004	INTEGRATED CHARGE PUMP DC/DC CONVERSION CIRCUITS USING THIN FILM TRANSISTORS	LIN, CHING-WEI
10767665	Not Issued	030	01/29/2004	PROCESS FOR FORMING POLYCRYSTALLINE SILICON LAYER BY LASER CRYSTALLIZATION	LIN, CHING-WEI
10709980	Not Issued	030	06/10/2004	METHOD OF FORMING A THIN FILM TRANSISTOR BY UTILIZING A LASER CRYSTALLIZATION PROCESS	LIN, CHING-WEI
10678908	Not Issued	041	10/03/2003	PROCESS FOR PASSIVATING POLYSILICON AND PROCESS FOR FABRICATING POLYSILICON THIN FILM	LIN, CHING-WEI

				TRANSISTOR	
09781431	6432758	150	02/13/2001	RECRYSTALLIZATION METHOD OF POLYSILICON FILM IN THIN FILM TRANSISTOR	LIN, CHING-WEI

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Lin **First Name** Ching-Wei Search

To go back use Back button on your browser toolbar.

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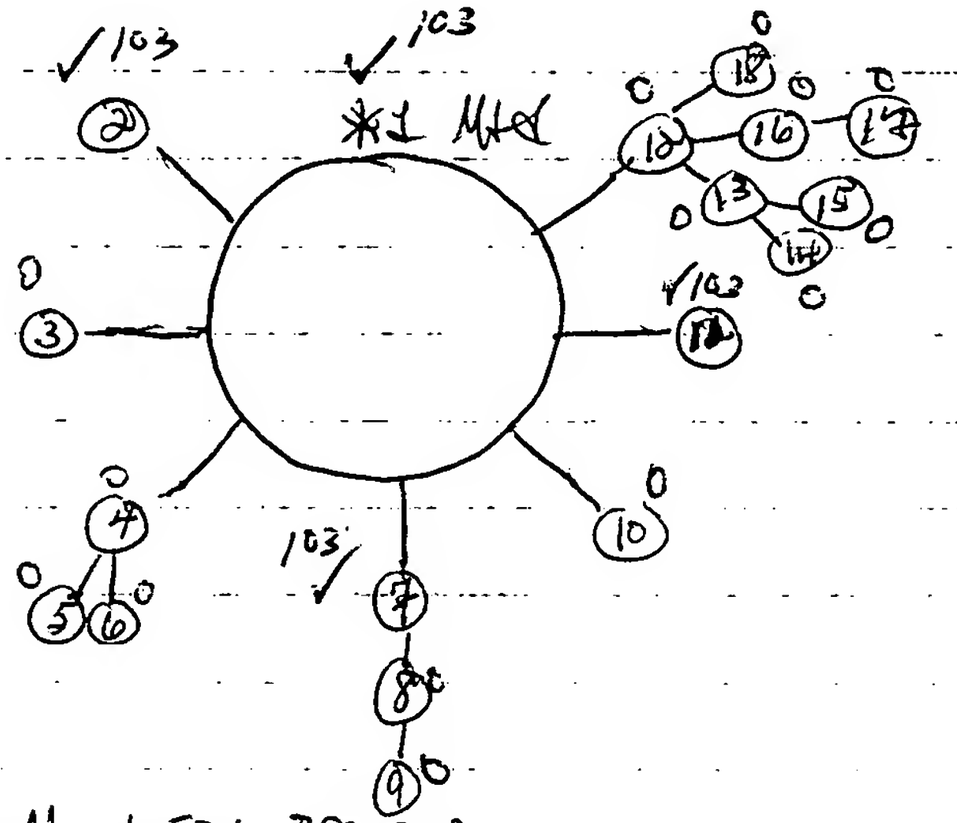
10/709,980 Examiner's Notes

~~LTFT or thin (w) film (w) transistor~~
~~LTPS TFT or low (w) temperature~~
S (LTFT or thin (w) film (w) transistor#
S (LTPS TFT or low (w) temperature (w) polysilicon (w) thin (w) film (w) transistor)
s (pattern?) (8a) (amorphous (8a) silicon or amorphous (8a) Si)
s (laser (8a) crystalize?)

Oath / Declaration
A No oath/declaration cite.



Ishida U.S. Pat No. 6,534,789 B2)

103 Rej
Claims 1, 2, 7 & 11

Object to:
Claims 3-6, 8-10 and 12-18.